MOSTEK®

ADD-IN MEMORY SYSTEMS

Technical Manual

MK8016
VAX 11/780*
ARRAY BOARD

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TABLE OF CONTENTS

SECTION **PAGE**

1.0 GENERAL DESCRIPTION 1
1.1 Introduction 1
1.2 Memory Specifications 1

2.0 INSTALLATION INFORMATION 3
2.1 Pre-Installation 3
2.2 Installation 3
2.3 Checkout of Memory Card 4

3.0 OPERATION 7
3.1 Introduction 7
3.2 Modes of Operation 7
3.2.1 Read/Write Operation 7
3.2.2 Refresh Mode 7
3.2.3 Initialize Mode 7

4.0 MAINTENANCE PROCEDURES 9
4.1 Introduction 9
4.2 Maintenance Philosophy 9
4.3 Preventive Maintenance 9
4.4 Troubleshooting Procedures 10

LIST OF TABLES AND FIGURES

TABLE **PAGE**

2.1 Interface Pin Assignments 4
4.1 Preventive Maintenance Schedule 9
4.2 Power Requirements 9
4.3 Array Board Address to Failing Board Translation 10
4.4 Memory Controller Syndrome/Bit Correlation 11
4.5 Array Key 11

FIGURE **PAGE**

4.1 Example Printout 12
4.2 Array Map 13
4.3 RAM Location Chart 14

1.0 GENERAL DESCRIPTION

1.1 INTRODUCTION

The MK8016 is a single card array designed for use in the VAX 11 780* family of computers.

The maximum capacity of a single card is 64K words by 72 bits. Each word consists of 64 data bits and eight ECC bits. This card is available in the following configurations:

32K Words x 72 Bits
64K Words x 72 Bits

The system uses up to 288 MK4116 or 288 MK4108 RAM devices. These devices are fabricated using Mostek's double-poly, N-Channel Silicon Gate POLY II process utilizing single transistor dynamic cells and dynamic circuitry throughout, including sense amplifiers to ensure that power dissipation is minimized.

1.2 MEMORY SPECIFICATIONS

(a)	Storage Capacity	64K Words Max Per Array Card
(b)	Word Length	72 Bits
(c)	Read Access Time	Compatible to VAX-1180 Memory Controller
(d)	Write Access Time	
(e)	Read Cycle Time	
(f)	Write Cycle Time	
(g)	Mode of Operation	Read Word Write Word Refresh Initialize
(j)	Input/Output	TTL Compatible
	Input Logic Levels	Low = –1.0V to +0.7V @ .2mA High = +2.7V to 5.5V @ 20mA
	Output Logic Levels	Low = –0.5V to +0.4V @ 12mA High = +2.4V to +5.25V @ 3mA
(k)	Data Input	72 Lines
(l)	Data Output	72 Lines
(m)	Input Controls	RASL, CASL, REFCYCH, INITH, READH
(n)	Input Address	19 Lines
(o)	Output Controls	BUS OUT SEL, BUS ENAB ARRAY OUT H
(p)	Temperature	0°C to 55°C Operating Ambient –40°C to 125°C Non-Operating
(q)	Relative Humidity	Up to 90% with no condensation
(r)	Altitude	10,000 ft. Operating 50,000 ft. Non-Operating
(s)	Input Power	+5V ± 5% @ 2.5 Amps Typical +12V ± 5% @ .13 Amps Typical
(t)	Dimensions	Each Card is 15.69" x 11.93" x .056"
(u)	Weight	2.2 Pounds Max Per Card

*VAX 11 780 is a trademark of Digital Equipment Corp.

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2.0 INSTALLATION INFORMATION

This section contains instructions for installing the MK8016 add-in array. Please read entire section before attempting the installation. This section is broken down into three parts as follows:

2.1 Pre-Installation
2.2 Installation
2.3 Checkout of Memory Card

2.1 PRE-INSTALLATION

Prior to arrival of board or boards, check for compliance with requirements as follows:

1. Adequate number of slots for boards ordered
2. Adequate power supply capacity for all units
3. Proper placement for individual units
4. Adequate equipment for checkout of system
   (a) Voltmeter (Simpson 260 or equivalent)
   (b) F.E. Tool Kit (Soldering iron, wire strippers, etc.)

2.2 INSTALLATION

2.2.1 Check all parts when received against shipping and ordering list. As you unpack materials inspect each unit for any shipping damage. Do not apply power to any unit which has been damaged.

2.2.2 Carefully check the card slot in which you intend to use the board.

2.2.3 Check all power pins with a voltmeter before plugging the board into its slot. The pins marked GND in Table 2.1 should read zero volts and the pins marked +5V in Table 2.1 should read +5%.

2.2.4 The MK8016 is an exact replacement for 1 or 2 M8210 memory board(s) and are installed as follows:

2.2.4.1 If you purchased a MK8016 populated with 288 MK4108 RAMs, the board replaces 1(one) M8210 memory board and should be inserted into the leftmost unoccupied memory slot. NOTE: all unused slots contain plastic "dummy" boards.

2.2.4.2 If you purchased a MK8016 populated with 288 MK4116 RAMs, the board replaces 2(two) M8210 memory boards and should be installed as follows:

The MK8016 and the jumper board will occupy two memory slots and must be paired as follows:

Slot 17 & 16
Slot 15 & 14
Slot 13 & 12
Slot 11 & 10
Slot 9 & 8
Slot 7 & 6
Slot 5 & 4
Slot 3 & 2

NOTE: The memory board and jumper board may be plugged into either slot but must be paired as indicated.

Example: If your memory controller contains 3 boards installed in 17, 16 & 15 and you desire to install a MK8016 fully populated with 4116 RAMs in the controller the following procedures should be followed:

1. Make all checks called out in paragraphs 2.1 & 2.2
2. Remove M8210 installed in 15 and the "dummy" boards in 14 & 13

3. Install the MK8016 and the jumper board in slots 15 & 14
4. Install the M8210 removed from 15 into 13
5. Save the "dummy" boards in case they should be required.

2.3 CHECKOUT OF MEMORY CARD

After installation, a complete on-line test should be run. The DEC memory diagnostics will provide an adequate check on the memory board. However, diagnostics should be run on all other components of the system also. If failure occurs refer to Sections 3 and 4 of this manual (Operation and Maintenance).

INTERFACE PIN ASSIGNMENTS
Table 2.1

DV2	Bus MOS Data U	Ø	BE1	Bus MOS Data L	8
DU2	Bus MOS Data U	1	BD1	Bus MOS Data L	9
DT2	Bus MOS Data U	2	BC1	Bus MOS Data L	10
DS2	↓	3	BB1	↓	11
ED1		4	BK1		12
EE1		5	BJ1		13
EF2		6	BH2		14
EH2		7	BF1	Bus MOS Data L	15
EJ2		8	BP1	Bus MOS Data 1	16
EK2		9	BN1	↓	17
EL2		10	BM1		18
EM2		11	BL1		19
ER2		12	BV2		20
ES2		13	BU2		21
EP2		14	BS1		22
EF1		15	BR1		23
EV2		16	CK2		24
EU1		17	CJ2		25
EU2		18	CM1		26
ET2		19	CK1		27
FJ2		20	CH2		28
FH2		21	CF2		29
FF2		22	CE2	↓	30
FE2		23	CD2	Bus MOS Data L	31
FP2		24	AJ1	Bus MOS Data C0	
FP1		25	AH2	Bus MOS Data C1	
FM2		26	AF1	↓ 2	
FL2		27	AE1	3	
FU2		28	DL1	4	
FY2		29	EB1	5	
FT2	↓	30	DP2	↓ 6	
FS2	Bus MOS Data U	31	DR2	Bus MOS Data C7	
AN1	Bus MOS Data L	0	DJ1	REFCYC H	
AM1	Bus MOS Data L	1	DL2	READ H	
AL1	Bus MOS Data L	2	DB1	INIT H	
AK1	↓	3	CD1	Bus Out SEL L	
BA1		4	EL1	Bus ENBL Array Out H	
AV2		5	FS1	Bus 4KL	
AU2		6	FR1	Bus 16KL	
AR1	Bus MOS Data L	7	FB2	Bus Mayu In XXL	
CU1	Slot Code LSB+3L	DA2	+5V Battery		
CN1	Array Addr 19H	DV1	+5V Battery		
CS1	Slot Code LSB + 2L	CA2	+5V Battery		

CONTINUED

INTERFACE PIN ASSIGNMENTS (Continued)

Table 2.1

CL2	Array Addr 18H	CV1	+5V Battery
CR1	Slot Code LSB + 1L	AV1	+5V
CP2	Array Addr 17H	BV1	+5V
CU2	Slot Code LSB L	EV1	+5V
CM2	Array Addr 16H	FV1	+5V
DM2	Array Addr 13H	AA2	+5V
DA1	Array CSL	BA2	+5V
DC1	Array Addr EXTH	EA2	+5V
DE1	Array Addr 12H	FA2	+5V
DK2	Array Addr 6H	FD2	+12V
DD1	Array Addr 11H	AS2	+12V
CT2	Array Addr 05H	FT1	GND
CS2	Array Addr 10H	ET1	GND
DH2	Array Addr 04H	FH1	GND
CR2	Array Addr 09H	EH1	GND
DJ2	Array Addr 03H	DH1	GND
DF2	Array Addr 08H	CH1	GND
CV2	Array Addr 02H	FC2	GND
DF1	Array Addr 07H	DT1	GND
DB2	Array Addr 01H	CT1	GND
CJ1	CAS L	BT1	GND
CP1	RAS L	AT1	GND
CL1	MUX Control H	BH1	GND
		AH1	GND
		AN2	GND
		AC2	GND
		BC2	GND
		BN2	GND
		CC2	GND
		CN2	GND
		DC2	GND
		DN2	GND
		EC2	GND
		EN2	GND
		FN2	GND
		BL2	-5V
		EK1	-5V

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3.0 OPERATION

3.1 INTRODUCTION

This section describes the modes of operation of the MK8016.

3.2 MODES OF OPERATION

The MK8016 is an array designed to operate in the VAX-11/780* Memory unit. It consists of an array supported by address, data drivers and receivers and a control logic section. It has four modes of operation: Read Word, Write Word, Refresh and Initialize. All operation modes described herein are totally VAX-11/780* compatible.

3.2.1 READ/WRITE OPERATION

The array, when reading or writing, receives addresses from the memory controller and compares the MSB's with a slot code provided by the backplane. If the board is selected the access continues. If the cycle is a read cycle, the data is placed on the memory bus under control of the VAX Memory Controller. If the cycle is a write cycle, the data is received, and driven into the array and is written under the control of the VAX Memory Controller.

The MK8016 may be fully populated with MK4116's or MK4108's or paritally populated with MK4116's

When fully populated with MK4108's or half populated with MK4116's the array represents 32K word x 72 or 256K byte capacity. In this configuration the MK8016 replaces one DEC M8210 array board.

When fully populated with MK4116's the MK8016 replaces two (2) DEC M8210 array boards. There are certain restrictions on the installation of these boards which is fully covered in paragraph 2.2.4.2. The adjacent slot as defined in that paragraph must have a jumper board installed to allow use of the additional memory devices or, if more arrays are plugged in higher slot numbers, to prevent indication of a configuration error.

3.2.2 REFRESH MODE

The MK8016 receives a signal from the memory address and control card which causes it to enable all RAS drivers to the array allowing a refresh operation to be performed under control of the VAX Memory Controller.

3.2.3 INITIALIZE MODE

The VAX memory controller has the capability to initialize or write known data with correct error correction code bits into the memory. It does this by asserting the Init line and writing data. The MK8016 receives the Init line uses it to allow initialization to proceed on the board. This signal asserts Board Select and enables the data drivers, RAS drivers, CAS drivers and Write signals to the array. Initialization is accomplished by writing in sequence to 16,384 address locations on the MK8016 regardless of the memory configuration.

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4.0 MAINTENANCE PROCEDURES

4.1 INTRODUCTION

This section contains the maintenance procedures required to keep the MK8016 array card in good running order. It includes:

1. A definition of the maintenance philosophy.
2. Preventive maintenance procedures.
3. Troubleshooting procedures.

4.2 MAINTENANCE PHILOSOPHY

The MK8016 requires little maintenance apart from periodic checking of the power supplies to make sure they meet the requirements specified in Table 4.2. In addition, the cooling system provided for the memory should be checked to make sure that an uninterrupted flow of clean air is supplied to the memory card. Troubleshooting is generally confined to isolating a faulty memory card in a multi-card configuration and to identifying a failing memory chip or chips.

CAUTION

DO NOT ATTEMPT TO REPAIR UNSOCKETED CARDS IN THE FIELD, SINCE SPECIAL HANDLING PROCEDURES ARE REQUIRED, FAULTY CARDS OR CHIPS SHOULD BE FLAGGED. THE CARD, DIAGNOSTIC PRINT OUT AND SYSTEM ERROR LOG REPORT SHOULD BE RETURNED TO THE FACTORY FOR REPAIR.

4.3 PREVENTIVE MAINTENANCE

The preventive maintenance needed to ensure satisfactory operation of the MK8016 is summarized in Table 4.1.

PREVENTIVE MAINTENANCE SCHEDULE
Table 4.1

FREQUENCY	CHECK	ACTION
Per Call	System Cooling Air Filter	Clean As Necessary
90 Days	Check System Power Supply Voltages	Adjust to Comply to Table 4.2
90 Days	Run DEC Diagnostic Program	Maintenance as Necessary

POWER REQUIREMENTS
Table 4.2

VOLTAGE
+5 VDC ± 5%
+12 VDC ± 5%
-5V VDC ± 5%

4.4 TROUBLESHOOTING PROCEDURES

Equipment needed for testing and maintaining the MK8016 is listed below:

1. Voltmeter - Simpson 260 or Equivalent
2. F.E. Tool Kit - Soldering Iron, Wire Strippers, Etc.
3. DEC Diagnostic Programs
4. DEC VMS System Software

If a problem arises in the memory the following general procedures should be observed:

1. Check the power supplies and make sure they comply with specifications in Section 4.3.
2. Make sure the card is properly mounted in its connector
3. Check for obvious causes of failure, such as faulty connectors, loose wires, etc.
4. Check inputs to the memory. I/O connections are listed in Table 2.2 (Interface Pin Assignments).
5. The DEC VMS Software contains error logging which may be examined by signing on to the system as the "System Manager", setting default to [SYSERR], renaming ERRLOG then running [SYS EXE] SYE with an S entered when options are requested. This results in an error log output which may be analyzed on the CRT or printed for permanent record.
6. The memory error print out of the error log or CRT display will resemble the example in Figure 4.1. Using this print out or display and the following procedure, RAM failures may be isolated and repaired in the field if the board is socketed. If the board is not socketed, it is recommended that it be returned to the factory for repair.
    a. Referring to the example print out in Figure 4.1 the A arrow points to the address of the failing board. The board referenced by this address may be determined by use of Table 4.3.
    b. The syndrome code is denoted by the B arrow in Figure 4.1. Refer to the syndrome code to data correlation table Table 4.4 and determine the bit in error.
    c. Refer to the array map illustrated in Figure 4.2 and determine the RAM locations for the failing data bit.
    d. Further isolation requires knowledge of board configurations or capacity. Table (4.5) gives the keys to isolate to the RAM level of the particular population type. The array bank is denoted by C arrow.
    e. Using this information go the RAM Location Chart Figure 4.3 to locate the faulty RAM(s).

ARRAY BOARD ADDRESS TO FAILING BOARD TRANSLATION TABLE
Table 4.3

Array Board Address	Board in Error
0	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	10
A	11
B	12
C	13
D	14
E	15
F	16

MEMORY CONTROLLER SYNDROME/BIT CORRELATION TABLE

Table 4.4

ERROR SYNDROME	FAILING BIT	ERROR SYNDROME	FAILING BIT
Ø1	CØ	8Ø	C7
Ø2	C1	89	UØ1
Ø4	C2	8A	UØ
Ø8	C3	8C	UØ4
1Ø	C4	8F	UØ7
19	LIØ	91	UØ9
1A	LØ2	92	U1Ø
1C	LØ4	94	U12
1F	LO/7	97	U15
2Ø	C5	98	U16
3B	LØØ	9B	U19
3B	LØ3	9D	U21
3D	LØ5	9E	U22
3E	LØ6	A8	UØØ
4Ø	C6	AB	UØ3
49	LØ9	AD	UØ5
4A	L1Ø	AE	UØ6
4C	L12	BØ	UØ8
4F	L15	B3	U11
51	L17	B5	U13
52	L18	B6	U14
54	L2Ø	B9	U17
57	L23	BA	U18
58	L24	BC	2Ø
5B	L27	BF	23
5D	L29	C1	25
5E	L3Ø	C2	26
68	LØ8	C4	28
6B	L11	C7	31
6D	L13	EØ	24
6E	L14	E3	27
7Ø	L16	E5	29
73	L19	E6	30
75	L21		
76	L22		
79	L25		
7A	L26		
7C	L28		
7E	L31		

CXX denotes check bit failure
UXX denotes data bit in upper half of long word
LXX denotes data bit in lower half of long word

ARRAY KEY

Table 4.5

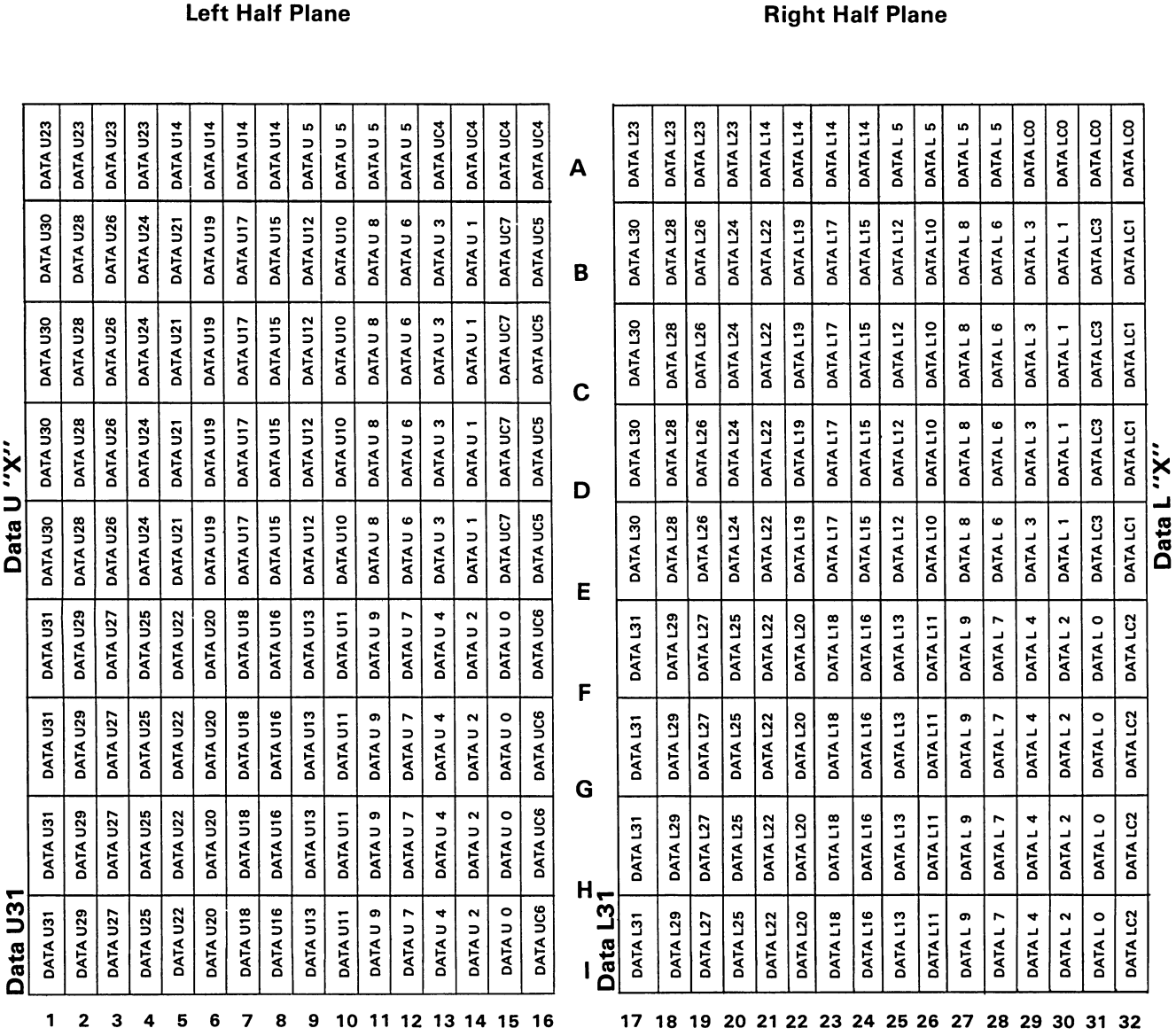
MK4116 Array Board	Array Bank In Error	MK4108 Populated (256KB)	MK4118 Full Pop. (512KB)	MK4116 Half Populated (256KB)
0, 2, 4, 6, 8, A C, E	Low Bank	3, 4	4	4
0, 2, 4, 6, 8, A C, E	Upper Bank	1, 2	2	2
1, 3, 5, 7, 9, B, D, F	Low Bank	3, 4	3	4
1, 3, 5, 7, 9, B, D, F	Upper Bank	1, 2	1	2

EXAMPLE PRINTOUT
Figure 4.1

```
29750     VAX/VMS              SYSTEM ERROR REPORT          COMPILED 16-NOV-1979 13:42
29760                                                                      PAGE 75.
29770
29780          PSL(ID#0F):     41F0000
29790                                                IPL<20:16>:                 1F
29800                                                PREVIOUS MODE <25:24>:      0
29810                                                    KERNEL
29820                                                CURRENT MODE<25:24>:        0
29830                                                    KERNEL
29840                                                EXECUTING ON INTERRUPT STACK<26>

29850     MEMORY CONTROLLER(S) REGISTERS:

29860     CONTROLLER 0:
29870          TR LEVEL:       1
29880          REGISTER A:     1610
29890                                                MEMORY TYPE:                2
29900                                                    16K CHIP BOARDS
29910                                                MEMORY SIZE (256KB INCR):   2.
29920                                                INTERLEAVE BITS<1:0>:
29930                                                    MEMORY NOT INTERLEAVED  0
29940          REGISTER B:     A0001000
29950                                                FILE READ ADDR. <31:30>:    2
29960                                                FILE WRITE ADDR. <29:28)>:  2
29970                                                START ADR (64KB INC) <27:15>: 0.
29980                                                MEMORY INIT. STATUS <13:12>: 1
29990                                                    MEMORY CONTAINS VALID DATA
30000                                                SUBSTITUTE ECC <07:00>:     0
30010          REGISTER C:     12328E58
30020                                                ERROR LOG REQUEST FLAG SET<28>
30030                                                ERROR ADDRESS <27:08>:  2328E
30040                                                    ARRAY BOARD <27:24>:    2 <-A
30050                                                    WORD IN ERROR <08>:     0
30060                                                      LOW WORD
30070                                                    CHIP ADDRESS <22:09>:  947
30080                                                    ARRAY BANK IN ERROR <23>: 0
30090                                                      LOW BANK <----------------C
30100                                                    ERROR SYNDROME <07:00>:  58 <-B
30110
30120

30130     * * * * * * * * * * * ENTRY 103. * * * * * * * * * * * * * * * * * * * *
30140     PERIODIC TIME STAMP                    LOGGED AT 4-DEC-1978 09:27:42.45
30150     ERROR SEQUENCE 456.                    ON PROCESSOR 0., SERIAL #FFFFFFFF
30160
30170

30180     * * * * * * * * * * * ENTRY 104. * * * * * * * * * * * * * * * * * * * *
30190     VOLUME MOUNTED                         LOGGED AT 4-DEC-1978 09:34:5000
30200     ERROR SEQUENCE 457.                    ON PROCESSOR 0., SERIAL #FFFFFFFF

30210     S              ON MIA0:
```

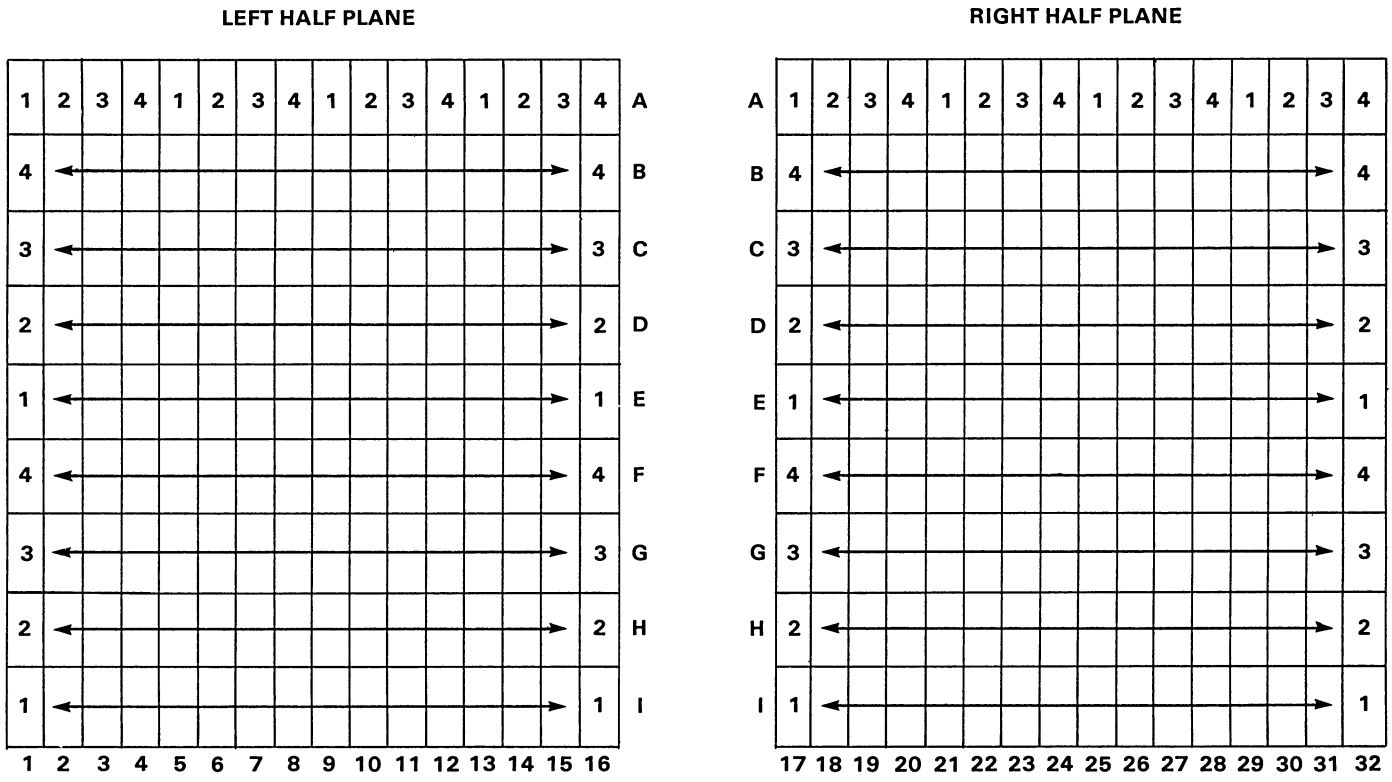
ARRAY MAP

Figure 4.2



RAM LOCATION CHART

Figure 4.3



EXAMPLE

Referring to Figure 4.1, and considering the MK8016 is half populated with MK4116's.

Translating the array board error (2) to array position ...

— Array board #3 is in error —

Bit location is determined by Syndrome (58)

— Bit L24 is in error —

Referring this to the Array Map, the RAMs in locations E20, D20, C20, and B20 are suspect.

Since this example is a MK4116 half populated board and the failure occurred in the Low Bank, Table 4.4 defines 4 as the key and referring this to Figure 4.3 we determine that RAM B20 must be replaced.

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